The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-32. (Canceled)

33. (Previously Presented) A semiconductor device including at least a pixel portion, a data line side driver circuit, a scanning line side driver circuit, and a memory portion, wherein,

said pixel portion is formed over a first substrate,

said data line side driver circuit and said memory portion are formed over a second substrate,

said scanning line side driver circuit is integrally formed over a third substrate,

said second substrate and said third substrate are provided in a region except for said pixel portion over said first substrate and are connected with said pixel portion such that a signal from said data line side driver circuit and a signal from said scanning line side driver circuit are input to the pixel region, and

the semiconductor device has a function for displaying an image in accordance with image data stored in said memory portion.

34. (Previously Presented) A semiconductor device according to claim 33, wherein said second substrate and said third substrate have the same thickness as said first substrate.

35. (Previously Presented) A semiconductor device according to claim 33, wherein said second substrate and said third substrate are made of the same material as said first substrate.

36. (Previously Presented) A semiconductor device according to claim 33, wherein said second substrate and said third substrate are one of a substrate having an insulating surface, an SOI substrate, and a silicon substrate.

37. (Previously Presented) A semiconductor device according to claim 33, wherein said semiconductor device has a function of displaying a still image in accordance with the image data stored in said memory portion.

38. (Previously Presented) A semiconductor device according to claim 33, wherein said semiconductor device includes a memory control circuit, and

said memory control circuit and said memory portion are formed over the same substrate.

39. (Previously Presented) A semiconductor device according to claim 33, wherein said semiconductor device is composed of a first region having a function of displaying the image and a second region having a function of supplying the image data to said first region,

said first region includes the substrate on which the pixel portion is formed, and

the semiconductor device includes a first display method of displaying the image in accordance with the image data supplied from said second region and a second display method of displaying the image in accordance with the image data stored in the memory portion provided in said first region.

40. (Previously Presented) A semiconductor device of claim 39, wherein power consumed in said semiconductor device by said second display method is 70 % or lower of power consumed in said semiconductor device by said first display method.

41. (Previously Presented) A semiconductor device of claim 39, wherein when said second display method is performed, 50 % or higher of power consumed in said semiconductor device is consumed in said first region.

42. (Previously Presented) A semiconductor device of claim 39, wherein when said second display method is performed, 90 % or higher of power consumed in said semiconductor device is consumed in said first region.

43. (Previously Presented) A semiconductor device of claim 39, wherein said first display method is controlled by a CPU provided in said second region,

said second display method is controlled by a control circuit provided in said first region, and

said second display method can be performed with a state in which a power source of said CPU is turned off.

44. (Previously Presented) A semiconductor device group composed of a first semiconductor device having a function of displaying an image and a second semiconductor device having a function of supplying image data to said first semiconductor device,

said first semiconductor device is a semiconductor device according to claim 33, wherein,

said semiconductor device group includes a first display method of displaying the image data supplied from said second semiconductor device and a second display method of displaying the image in accordance with the image data stored in the memory portion included in said first semiconductor device.

45.-54. (Canceled)

55. (Currently Amended) A device comprising:

a pixel portion over a substrate;

a data line side driver circuit provided over the substrate and operationally connected to the pixel portion;

a memory portion provided over the substrate and operationally connected to the data line side driver circuit;

a memory control circuit provided over the substrate and operationally connected to the memory portion wherein an image signal is transferred ~~in a direction~~ to said memory control circuit, from said memory control ~~circuit,~~ circuit to said memory portion, and from said memory portion to said data line side driver circuit.

56. (Previously Presented) The device according to claim 55 wherein said memory is selected from the group consisting of SRAM, DRAM, and EEPROM.

57. (Currently Amended) A device comprising:

a pixel portion over a substrate;

a data line side driver circuit provided over the substrate and operationally connected to the pixel portion;

a memory portion provided over the substrate and operationally connected to the data line side driver circuit;

a memory control circuit provided over the substrate and operationally connected to the memory portion and the data line side driver circuit wherein an image signal is transferred ~~in a direction~~ to said memory control circuit, from said memory control ~~circuit,~~ circuit to said memory portion, and from said memory portion to said data line side driver circuit.

58. (Previously Presented) The device according to claim 57 wherein said memory is selected from the group consisting of SRAM, DRAM, and EEPROM.

59. (Previously Presented) A device comprising:

an input terminal;

a first control circuit operationally connected to the input terminal;

a second control circuit operationally connected to the first control circuit;

at least one first memory operationally connected to the first control circuit;

a memory control circuit operationally connected to the second control circuit;

a memory portion operationally connected to the memory control circuit;

a data line side driver circuit operationally connected to the memory portion; and

a pixel portion operationally connected to the data line side driver circuit,

wherein all of the first control circuit, the second control circuit, the first memory, the memory control circuit, the memory portion, the data line side driver circuit and the pixel portion are provided adjacent to a same substrate.

60. (Previously Presented) The device according to claim 59 wherein said memory is selected from the group consisting of SRAM, DRAM, and EEPROM.